IN THE CLAIMS:

Please amend the claims as follows:

1. (Canceled)

2. (Previously Presented) A method of reducing skew between rising and falling data at an output node of a buffer circuit, comprising:

generating an intermediate voltage signal from an input voltage signal applied to an input node of the buffer circuit;

generating an output voltage signal at the output node based on the intermediate voltage signal; and

coupling a first compensating current source between a supply voltage line and the output node to compensate for changes in NMOS current drive, wherein the first compensating current source comprises a current source transistor for delivering a compensating current to the output node, the current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

3. (Previously Presented) The method of claim 2, further comprising coupling a second compensating current source between the output node and ground to compensate for changes in PMOS current drive.

4. (Previously Presented) A method of reducing skew between rising and falling data at an output node of a buffer circuit, comprising:

generating an intermediate voltage signal from an input voltage signal applied to an input node of the buffer circuit;

generating an output voltage signal at the output node based on the intermediate voltage signal;

coupling at least one compensating current source to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged; and

controlling the amount of current provided by the compensating current source via a process dependent current source whose current is mirrored to the output node by the compensating current source.

5. (Original) The method of claim 4, further comprising controlling the amount of current supplied by the compensating current source via a relatively process independent bias voltage applied to a gate of a transistor of the process dependent current source.

6-7. (Canceled)

8. (Previously Presented) A buffer circuit, comprising:

a first stage for generating an intermediate voltage signal from an input voltage signal applied to an input node of the first stage;

a second stage to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the first compensating current source comprises a first current source transistor to supplement current flowing into the output node through the PMOS transistor as function of NMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

9. (Original) The buffer of claim 8, wherein changes in current provided by the first current source are proportional to changes in current through the NMOS transistor.

10. (Original) The buffer circuit of claim 8, further comprising at least a second current source to supplement current flowing from the output node through the NMOS transistor as function of PMOS current drive.

11. (Previously Presented) A buffer circuit, comprising:

a first stage for generating an intermediate voltage signal from an input voltage signal applied to an input node of the first stage;

a second stage to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the first compensating current source comprises a first current source transistor, a current flowing through the first current source transistor supplementing a current flowing from the output node through the NMOS transistor as function of PMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

12. (Original) The buffer of claim 11, wherein changes in current provided by the first compensating current source are proportional to changes in current through the PMOS transistor.

13. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node, the second branch delivering a current to the output node, wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch.

14. (Previously Presented) The buffer circuit of claim 13, wherein:

current flowing through the first branch of the first current mirror circuit varies with changes to the NMOS current drive; and

current flowing from the second branch of the first current mirror circuit supplements current flowing into the output node through the PMOS transistor.

15. (Previously Presented) The buffer circuit of claim 13, wherein:

current flowing through the first branch of the first current mirror circuit varies with changes to the PMOS current drive; and

current flowing into the second branch of the first current mirror circuit supplements current flowing from the output node through the NMOS transistor.

16. (Original) The buffer of claim 15, further comprising at least a second current mirror circuit having a first branch and a second branch coupled with the output node, wherein:

current flowing through the first branch of the second current mirror circuit varies with changes to NMOS current drive; and

current flowing from the second branch of the second current mirror circuit supplements current flowing into the output node through the PMOS transistor.

17. (Original) The buffer circuit of claim 13, wherein the current flowing through the first branch of the first current mirror circuit is set by a process independent bias voltage supplied to a gate of a process dependent transistor.

18. (Original) The buffer circuit of claim 13, wherein the second branch of the first current mirror circuit comprises an NMOS transistor in parallel with the NMOS transistor of the inverter stage.

19. (Original) The buffer circuit of claim 13, wherein the second branch of the first current mirror circuit comprises a PMOS transistor in parallel with the PMOS transistor of the inverter stage.

20-21. (Canceled)

22. (Previously Presented) A memory device, comprising:

an input to receive an external clock signal; and

a buffer circuit for generating an internal clock signal to be provided to one or more components of the memory device, wherein the buffer circuit comprises a first stage for generating an intermediate voltage signal indicative of a difference between a reference voltage signal and the clock signal, a second stage for generating an output voltage signal on an output node based on the intermediate voltage signal, an inverter for generating the internal clock signal based on the output voltage signal, and at least one compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the at least one compensating current source comprises a first current source transistor to supplement current flowing into the output node through the PMOS transistor as function of NMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

23. (Original) The memory device of claim 22, wherein the at least one compensating current source further comprises a second current source to supplement current flowing from the output node through the NMOS transistor as function of PMOS current drive.

24. (Previously Presented) A memory device, comprising:

an input to receive an external clock signal; and

a buffer circuit for generating an internal clock signal to be provided to one or more components of the memory device, wherein the buffer circuit comprises a first stage for generating an intermediate voltage signal indicative of a difference between a reference voltage signal and the clock signal, a second stage for generating an output voltage signal on an output node based on the intermediate voltage signal, an inverter for generating the internal clock signal based on the output voltage signal, and at least one compensating current source coupled to the output node to compensate for

changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the at least one compensating current source comprises a first current source transistor, a current flowing through the first current source transistor supplementing current flowing from the output node through the NMOS transistor as function of PMOS current drive, the first current source transistor having a control terminal which is controlled independent on the intermediate voltage signal.

25. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor;

at least a first current mirror circuit having a first branch and a second branch coupled to the output node, wherein:

current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch,

wherein current flowing through the first branch of the first current mirror circuit varies with changes to the PMOS current drive, and

wherein current flowing into the second branch of the first current mirror circuit supplements current flowing from the output node through the NMOS transistor; and

at least a second current mirror circuit having a first branch and a second branch coupled with the output node, wherein:

current flowing through the first branch of the second current mirror circuit varies with changes to NMOS current drive; and

current flowing from the second branch of the second current mirror circuit supplements current flowing into the output node through the PMOS transistor.

26. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node,

wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch, and

wherein the second branch of the first current mirror circuit comprises an NMOS transistor in parallel with the NMOS transistor of the inverter stage.

27. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node,

wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch,

wherein the second branch of the first current mirror circuit comprises a PMOS transistor in parallel with the PMOS transistor of the inverter stage.

28. (New) The method of claim 2, wherein the compensating current is delivered to the output node through the current source transistor.

29. (New) The buffer of claim 8, wherein current flows through the first current source transistor to supplement current flowing into the output node.

30. (New) The buffer circuit of claim 13, wherein a transistor of the second branch delivers current to the output node.

31. (New) The memory device of claim 22, wherein a current flows through the first current source transistor to supplement current flowing into the output node.